

### **REMARKS**

Applicant appreciates the detailed examination evidenced by the Office Action mailed March 27, 2008 (hereinafter "Office Action"). In response thereto, Applicant respectfully requests entry of the amendments in which Claim 10 is amended, Claims 1-5 and 28-30 are canceled and New Claim 31 is added. Claims 10 and 31 are presently pending in the application. Applicant respectfully submits that all claims are in condition for allowance for at least the reasons stated below.

#### **Drawing objections are overcome**

The Office Action objects to the drawings under 37 C.F.R. §1.83(a) as not showing every feature of the invention specified in the claims. Specifically, the Office Action states that:

Claim 1 recited the limitation "a sidewall of the hole" in lines 3, 5 & 8. It is not clear as to where in the drawings (Applicant's Fig. 7-8) the sidewall is positioned. In applicant's Fig. 7, is the sidewall directly contacting silicon oxide layer 452a or the sidewall is directly contacting silicon nitride layer 454a? The same ambiguity surrounding "sidewall" exists in applicant's Fig. 8. This limitation must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Office Action, page 2. Applicant respectfully submits that Claim 1 is canceled herein and thus the objections to the drawings are moot.

#### **Section 112 Rejections**

The Office Action rejects Claims 1 and 10 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claims the subject matter which applicant regards as the invention. Office Action, page 3. Regarding Claim 1, Applicant respectfully submits that Claim 1 is canceled and thus the rejection of Claim 1 is moot.

Regarding Claim 10, the Office Action states that "Claim 10 recites the limitation "[t]he sidewall of the contact hole" in line 10. There is insufficient antecedent basis for this limitation in the claim." Office Action, page 3. Applicant respectfully submits that Claim 10 is amended to overcome the insufficient antecedent basis issue identified in the Office Action.

The Office Action also states that Claim 10 "recites the limitation 'gate line patterns' in line 4. It is not clear as to what elements within a gate structure this limitation include." Office Action, page 3. Applicant respectfully submits that some embodiments provide that "the conductive line pattern 330 is a gate line pattern or a bit line pattern." Specification, page 7, lines 16-17. In some embodiments, "[t]ransistors, which include source/drain regions, and gate line patterns 412 are formed in and on the silicon substrate 400." Specification, page 8, lines 16-17. Applicant respectfully submits that the cited portions of the Specification in combination with the respective drawings should provide sufficient clarification regarding what elements in a gate structure include gate line patterns. Accordingly, Applicant respectfully submits that the rejections under 35 U.S.C. §112, second paragraph, are overcome and requests withdrawal thereof.

**Claim 10 is patentable over Koga, Igarashi and Yokoyama**

The Office Action states that Claim 10 is rejected under 35 U.S.C. §103(a) as being unpatentable over Koga in view of Igarashi and in further view of U.S. Patent No. 6,703,715 to Yokoyama ("Yokoyama"). Office Action, page 7. Applicant respectfully traverses the rejection on the basis that Koga, Igarashi and Yokoyama, alone or in combination, do not disclose or suggest all of the recitations of Claim 10. For example, Claim 10, as amended, recites:

An integrated circuit device comprising:  
an integrated circuit substrate in which source/drain regions are formed;  
a first interlevel dielectric layer which is formed on the integrated circuit substrate;  
***gate line patterns which are formed in the first interlevel dielectric layer;***  
contact pads which are ***present between adjacent gate line patterns in the first interlevel dielectric layer*** and electrically connected to the source/drain regions;  
a second interlevel dielectric layer which is formed on the first interlevel dielectric layer, wherein contact holes, through which the contact pads are exposed, are formed in the second interlevel dielectric layer;  
first contact spacers which are formed along the side walls of the contact holes, the first contact spacers being formed of silicon oxide;  
second contact spacers which are formed of silicon nitride and formed on the first contact spacers; and  
contact plugs which are present in the contact holes between the second contact spacers,

wherein the conductive contact contacts the contact pad, wherein the first spacer extends along the side wall to contact the contact pad and ***wherein the second spacer does not contact the contact pad.***

(*Emphasis added.*) As an initial matter, Applicant respectfully submits that Igarashi appears to teach away from the portions cited in the Office Action in that those portions are directed to background methods, deficiencies of which Igarashi appears to be trying to overcome. For example, regarding the silicide described in Igarashi, in one of the recitations upon which the Office Action bases its rejection, Igarashi appears to identify "problems of increased writing resistance and unstable resistance when silicide is formed so arise." Igarashi, column 3, lines 48-50. Thus, in addition to lacking a motivation to combine the cited portions of Igarashi (e.g., Fig. 16), Igarashi appears to teach away from the structures/methods described in the portions cited in the Office Action.

As a general matter, a structure according to the recitations of Claim 10 is so distinctive from Koga, Igarashi and Yokoyama, alone or in combination, that selecting various elements therefrom without limitation, motivation or suggestion still fails to disclose or suggest the recitations of Claim 10. Moreover, the recitations of Claims 10 and 31 are more directed to metallization level structures in contrast with the references, which appear to be directed to gate level structures.

In rejecting Claim 10, the Office Action states, in part, that Koga teaches "gate line patterns 203 which are formed in the first interlevel dielectric layer." Office Action, page 7. Applicant respectfully submits that, in contrast with gate line patterns, as recited in Claim 10, Koga appears to describe a gate electrode 200 formed of a "cap film 205, WSi film 204, and polysilicon film 203." Koga, column 1, lines 36-38. Thus, in contrast with the Office Action allegation, Koga does not disclose or suggest "gate line patterns which are formed in the first interlevel dielectric layer," as recited in Claim 10.

The Office Action further states that:

[h]owever, Koga does not explicitly teach contact pads between adjacent gate line patterns and connected to the source/drain regions. Nonetheless, Igarashi teaches in figure 16, wherein a silicide contact pad 105 is positioned to make an ohmic contact with a diffusion layer 104 underneath...it would have been obvious to a person of ordinary skill in the art to modify Koga by using a silicide contact pad as taught by Igarashi in the interest of an ohmic contact with the diffusion layer 208 underneath.

Office Action, pages 7-8. The Applicant respectfully submits that even if one would be motivated to modify Koga using the silicide film 105 of Igarashi, the resulting contact pads would not be "present between adjacent gate line patterns **in the first interlevel dielectric layer**," as recited in Claim 10. For example, Igarashi appears to provide that "a silicide film 5 is formed in the impurity diffusion layer 4." Column 10, lines 53-54 and Figure 6. In this regard, even if the silicide film 5 may be interpreted as a contact pad, Igarashi does not disclose or suggest that the silicide film 5 would be "present between adjacent gate line patterns **in the first interlevel dielectric layer**," as recited in Claim 10.

In contrast with the Office Action allegation, Koga, Igarashi and Yokoyama, alone or in combination, do not disclose or suggest "wherein the conductive contact contacts the contact pad, wherein the first spacer extends along the side wall to contact the contact pad and wherein the second spacer does not contact the contact pad," as recited in Claim 10. Applicant respectfully submits that some embodiments according to Claim 10 may be illustrated in Figure 8 in that a first spacer 452a contacts a contact pad 415 and a second spacer 454a does not contact the contact pad 415. Applicant respectfully submits that even if, as the Office Action alleges, a silicide contact pad were used in Koga's device, a contact pad that covers the entire surface underneath the conductive contact 106 would not include a first spacer that "extends along the side wall to contact the contact pad" and a second spacer that "does not contact the contact pad," as recited in Claim 10.

Moreover, there is no suggestion or motivation to modify Koga by including the contact pad described in Igarashi. For example, there would be no motivation to provide a contact pad between the source and drain regions 208 and the electrode 213a in the context of an insulated field effect transistor described in Koga. Thus, for at least these reasons, Koga, Igarashi and Yokoyama, alone or in combination, do not disclose or suggest several of the recitations of Claim 10. Accordingly, Claim 10 is patentable over Koga, Igarashi and Yokoyama for at least these reasons.

#### **New Claim 31 is patentable**

Applicant respectfully submits that new Claim 31 is patentable for at least the reason that the art of record does not disclose or suggest the recitations therein. For example, Claim 31 recites, in part "wherein the conductive contact contacts the contact pad, wherein the first

spacer extends along the side wall to contact the contact pad and wherein the second spacer does not contact the contact pad." As discussed above regarding Claim 10, the art of record does not disclose or suggest the first spacer that "extends along the side wall to contact the contact pad" and the second spacer that "does not contact the contact pad," as recited in Claim 31. Accordingly, Claim 31 is patentable over the art of record for at least these reasons.

In re: Beom-jun Jin  
Serial No.: 10/689,981  
Filed: October 20, 2003  
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### CONCLUSION

As all of the claims are now in condition for allowance, Applicants respectfully request allowance of the claims and passing of the application to issue in due course. Applicants urge the Examiner to contact Applicants' undersigned representative at (919) 854-1400 to resolve any remaining formal issues.

Respectfully submitted,

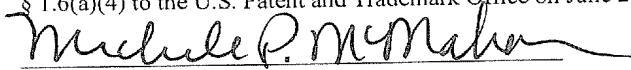


Timothy J. Wall  
Registration No. 50,743

**USPTO Customer No. 20792**  
Myers Bigel Sibley & Sajovec  
Post Office Box 37428  
Raleigh, North Carolina 27627  
Telephone: 919/854-1400  
Facsimile: 919/854-1401

### CERTIFICATION OF TRANSMISSION

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Michele P. McMahan